What is claimed is:

1. A method of forming a portion of a NAND memory array, comprising:

forming a select line coupled to each of a plurality of NAND strings of memory cells of the memory array, wherein the select line comprises a select gate at each intersection of one of the plurality of NAND strings and the select line; wherein forming the select line comprises:

connecting first and second conductive layers of the select line that are separated by an interlayer dielectric using a contact that extends from a third conductive layer, formed on the second conductive layer, to the first conductive layer, the contact formed in a hole that passes through the second conductive layer and the interlayer dielectric layer and that terminates at the first conductive layer.

2. The method of claim 1, wherein the hole is slot that spans the plurality of NAND strings so that the contact spans the plurality of NAND strings.

3. The method of claim 1, wherein the hole is substantially aligned with an isolation region of the memory array.

4. The method of claim 1, wherein the first and second conductive layers are polysilicon layers and the third conductive layer is a metal-containing layer.

5. The method of claim 1, further comprising forming the first conductive layer on a dielectric layer overlying a substrate.

6. The method of claim 1, wherein forming a select line further comprises forming a source select line and a drain select line at opposite ends of each NAND string, wherein the source select line comprises a source select gate at each intersection of one of the plurality of NAND strings and the source select line, and the drain select line comprises a drain select gate at each intersection of one of the plurality of NAND strings and the drain select line.

7. A method of forming a portion of a NAND memory array, comprising:

forming a plurality of NAND strings of memory cells;

forming a select line coupled to each of the NAND strings, wherein the select line comprises a select gate at each intersection of one of the plurality of NAND strings and the select line, wherein forming the select line comprises:

forming first and second conductive layers with an interposing dielectric layer; and

electrically connecting the first and second conductive layers, wherein electrically connecting the first and second conductive layers comprises:

forming a hole through the second conductive layer and the interlayer dielectric layer that terminates at the first conductive layer so as to expose a portion of the first conductive layer; and

forming a third conductive layer on the second conductive layer and on sidewalls of the hole and the exposed portion of the first conductive layer to form a contact in the hole that electrically connects the first and second conductive layers.

8. The method of claim 7, wherein forming the hole further comprises forming a slot-shaped hole that spans two or more NAND strings of the plurality of NAND strings.

9. The method of claim 7, wherein forming the hole further comprises substantially aligning the hole with an isolation region of the memory array.

10. The method of claim 7, wherein the first and second conductive layers are polysilicon layers and the third conductive layer is a metal-containing layer.

11. The method of claim 7, further comprising forming the first conductive layer on a second dielectric layer overlying a substrate.

12. A method of forming a portion of a NAND memory array, comprising:

forming a plurality of NAND strings of memory cells;

forming a select line coupled to each of the NAND strings, wherein the select line comprises a select gate at each intersection of one of the plurality of NAND strings and the select line, wherein forming the select line comprises:

forming a first dielectric layer on a substrate;

forming a first conductive layer on the first dielectric layer;

forming a second dielectric layer on the first conductive layer;

forming a second conductive layer on the second dielectric layer;

patterning the second conductive layer to expose a portion of the second conductive layer;

removing the exposed portion of the second conductive layer and a portion of the second dielectric layer directly underlying the exposed portion of the second conductive layer to form a hole that passes through the second conductive layer and second dielectric layer and that terminates at the first conductive layer, thereby exposing a portion of the first conductive layer; and

forming a third conductive layer on the second conductive layer and on sidewalls of the hole and the exposed portion of the first conductive layer to form a contact in the hole that electrically connects the first and second conductive layers.

13. The method of claim 12, wherein the hole is a slot that spans two or more NAND strings of the plurality of NAND strings so that the contact spans the two or more NAND strings of the plurality of NAND strings.

14. The method of claim 12, wherein forming the hole further comprises substantially aligning the hole with an isolation region formed in the substrate.

15. The method of claim 12, wherein the first and second conductive layers are polysilicon layers and the third conductive layer is a metal-containing layer.

16. The method of claim 15, wherein metal-containing layer comprises a material selected from the group consisting of refractory metals and refractory metal silicides.

17. The method of claim 12, wherein forming a select line further comprises forming a source select line and a drain select line at opposite ends of each NAND string,

wherein the source select line comprises a source select gate at each intersection of one of the plurality of NAND strings and the source select line, and the drain select line comprises a drain select gate at each intersection of one of the plurality of NAND strings and the drain select line.

18. A method of forming a portion of a NAND memory array, comprising:

forming a plurality of NAND strings of memory cells;

forming a select line coupled to each of the NAND strings, wherein the select line comprises a select gate at each intersection of one of the plurality of NAND strings and the select line, wherein forming the select line comprises:

forming a first dielectric layer on a substrate;

forming a first polysilicon layer on the first dielectric layer;

forming a second dielectric layer on the first polysilicon layer;

forming a second polysilicon layer on the second dielectric layer;

patterning the second polysilicon layer to expose a portion of the second polysilicon layer;

removing the exposed portion of the second polysilicon layer and a portion of the second dielectric layer directly underlying the exposed portion of the second polysilicon layer to form a hole that is substantially aligned with an isolation region formed in the substrate, that passes through the second polysilicon layer and second dielectric layer, and that terminates at the first polysilicon layer, thereby exposing a portion of the first polysilicon layer; and

forming a metal-containing layer on the second polysilicon layer and on sidewalls of the hole and the exposed portion of the first polysilicon layer to form a contact in the hole that electrically connects the first

and second polysilicon layers and that substantially aligns with the isolation region.

19. A method of forming a portion of a NAND memory array, comprising:

forming a plurality of NAND strings of memory cells;

forming a select line coupled to each of the NAND strings, wherein the select line comprises a select gate at each intersection of one of the plurality of NAND strings and the select line, wherein forming the select line comprises:

forming a first dielectric layer on a substrate;

forming a first polysilicon layer on the first dielectric layer;

forming asecond dielectric layer on the first polysilicon layer;

forming a second polysilicon layer on the second dielectric layer;

patterning the second polysilicon layer to expose a portion of the second polysilicon layer;

removing the exposed portion of the second polysilicon layer and a portion of the second dielectric layer directly underlying the exposed portion of the second polysilicon layer to form a slot that spans two or more NAND strings of the plurality of NAND strings, that passes through the second polysilicon layer and second dielectric layer, and that terminates at the first polysilicon layer, thereby exposing a portion of the first polysilicon layer; and

forming a metal-containing layer on the second polysilicon layer and on sidewalls of the slot and the exposed portion of the first polysilicon layer to form a contact in the slot that electrically connects the first and second polysilicon layers and that spans the two or more NAND strings of the plurality of NAND strings.

20. A NAND memory array comprising:

a select line coupled to each of a plurality of NAND strings of memory cells of the memory array, wherein the select line comprises a select gate at each intersection of one of the plurality of NAND strings and the select line; wherein the select line further comprises:

first and second conductive layers separated by a dielectric layer; and

a contact that extends from a third conductive layer, disposed on the second conductive layer, to the first conductive layer, the contact formed in a hole that passes through the second conductive layer and the dielectric layer and that terminates at the first conductive layer, the contact electrically connecting the first and second conductive layers.

21. The NAND memory array of claim 20, wherein the hole is a slot that spans two or more NAND strings of the plurality of NAND strings so that the contact spans the two or more NAND strings of the plurality of NAND strings.

22. The NAND memory array of claim 20, wherein the contact is substantially aligned with an isolation region of the memory array.

23. The NAND memory array of claim 20, wherein the first and second conductive layers are polysilicon layers and the third conductive layer is a metal-containing layer.

24. The NAND memory array of claim 23, wherein the metal-containing layer comprises a material selected from the group consisting of refractory metals and refractory metal silicides.

25. The NAND memory array of claim 20, wherein the first conductive layer is disposed on a second dielectric layer overlying a substrate.

26. The NAND memory array of claim 20, wherein the contact is integral with the third conductive layer.

27. A NAND memory array comprising:

a plurality of NAND strings of memory cells;

a select line coupled to each of the NAND strings of memory cells, wherein the select line comprises a select gate at each intersection of one of the plurality of NAND strings and the select line; wherein the select line further comprises:

a first dielectric layer disposed on a substrate;

a first conductive layer disposed on the first dielectric layer;

a second dielectric layer disposed on the first conductive layer;

a second conductive layer disposed on the second dielectric layer;

a third conductive layer disposed on the second conductive layer; and

a contact that extends from the third conductive layer to the first conductive layer, the contact formed in a hole that passes through the second conductive layer and the second dielectric layer and that terminates at the first conductive layer, the contact electrically connecting the first and second conductive layers.

28. The NAND memory array of claim 27, wherein the hole is a slot that spans two or more NAND strings of the plurality of NAND strings so that the contact spans the two or more NAND strings of the plurality of NAND strings.

29. The NAND memory array of claim 27, wherein the contact is substantially aligned with an isolation region disposed in the substrate.

30. The NAND memory array of claim 27, wherein the first and second conductive layers are polysilicon layers and the third conductive layer is a metal-containing layer.

31. The NAND memory array of claim 27, wherein the contact is integral with the third conductive layer.

32. A NAND memory array comprising:

a plurality of NAND strings of memory cells;

a select line coupled to each of the NAND strings of memory cells, wherein the select line comprises a select gate at each intersection of one of the plurality of NAND strings and the select line; wherein the select line further comprises:

a first dielectric layer disposed on a substrate;

a first polysilicon layer disposed on the first dielectric layer;

a second dielectric layer disposed on the first polysilicon layer;

a second polysilicon layer disposed on the second dielectric layer;

a metal-containing layer disposed on the second polysilicon layer; and

a contact internal to the select line that substantially aligns with an isolation region formed in the substrate and that extends from the metal-containing layer, passes through the second polysilicon layer and the second dielectric layer, and terminates at the first polysilicon layer, the contact electrically connecting the first and second polysilicon layers.

33. A NAND memory array comprising:

a plurality of NAND strings of memory cells;

a select line coupled to each of the NAND strings of memory cells, wherein the select line comprises a select gate at each intersection of one of the plurality of NAND strings and the select line; wherein the select line further comprises:

a first dielectric layer disposed on a substrate;

a first polysilicon layer disposed on the first dielectric layer;

a second dielectric layer disposed on the first polysilicon layer;

a second polysilicon layer disposed on the second dielectric layer;

a metal-containing layer disposed on the second polysilicon layer; and

a contact internal to the select line that spans two or more NAND strings of the plurality of NAND strings and that extends from the metal-containing layer, passes through the second polysilicon layer and the second dielectric layer, and terminates at the first polysilicon layer, the contact electrically connecting the first and second polysilicon layers.

34. A memory device comprising:

a memory array comprising:

a plurality of rows of memory cells; and

a plurality of columns, each column comprising a NAND string of memory cells coupled between a source select line and a drain select line, wherein the source select line comprises a source select gate at each intersection of one of the NAND strings and the drain select line comprises a drain select gate at each intersection of one of the NAND strings and the drain select line, the source and drain select lines further comprising:

first and second conductive layers separated by a dielectric layer; and

a contact that extends from a third conductive layer, disposed on the second conductive layer, to the first conductive layer, the contact formed in a hole that passes through the second conductive layer and the dielectric layer and that terminates at the first conductive layer, the contact electrically connecting the first and second conductive layers;

column access circuitry coupled to the columns; and

row access circuitry coupled to the rows.

35. The memory device of claim 34, wherein the hole is a slot that spans two or more columns of the plurality of columns so that the contact spans the two or more columns of the plurality of columns.

36. The memory device of claim 34, wherein the hole is substantially aligned with an isolation region of the memory array.

37. A memory device comprising:

a memory array comprising:

a plurality of rows of memory cells; and

a plurality of columns, each column comprising a NAND string of memory cells coupled between a source select line and a drain select line, wherein the source select line comprises a source select gate at each intersection of one of the NAND strings and the source select line and the drain select line comprises a drain select gate at each intersection of one of the NAND strings and the drain select line, the source and drain select lines further comprising:

a first dielectric layer disposed on a substrate;

a first conductive layer disposed on the first dielectric layer;

a second dielectric layer disposed on the first conductive layer;

a second conductive layer disposed on the second dielectric layer;

a third conductive layer disposed on the second conductive layer; and

a contact that extends from the third conductive layer to the first conductive layer, the contact formed in a hole that passes through the second conductive layer and the second dielectric layer and that terminates at the first conductive layer, the contact electrically connecting the first and second conductive layers;

column access circuitry coupled to the columns; and

row access circuitry coupled to the rows.

38. The memory device of claim 37, wherein the hole is a slot that spans two or more columns of the plurality of columns so that the contact spans the two or more columns of the plurality of columns.

39. The memory device of claim 37, wherein the contact is substantially aligned with an isolation region disposed in the substrate.